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RS–232 ↔ IEEE 488 INTERFACE CONVERTER

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SECTION 1

INTRODUCTION

1.1 DESCRIPTION

The Interface Converter provides transparent communication from an RS-232C computer to an IEEE 488 printer, plotter or other device. It also can be used to control an RS-232C device, such as a printer or terminal, from an IEEE 488 host computer.

As an RS-232C to IEEE 488 converter, the Interface Converter receives data from an RS-232C host computer. It then automatically performs the bus sequences necessary to send this data to the IEEE 488 device. If desired, data can be requested from the IEEE 488 device and returned to the host.

As an IEEE 488 to RS-232C converter, the Interface Converter is a peripheral to an IEEE 488 controller. Data received from the controller is sent to the RS-232C device, and data received from the RS-232C device is buffered for transmission to the IEEE 488 controller. The Interface Converter can inform the host, by issuing a Service Request, that it has received data from the serial device.

1.2 SPECIFICATIONS

Serial Interface

EIA RS-232C: 7(AB), 2(BA), 3(BB), 4(CA), 5(CB)
Character Set: Asynchronous bit serial
Duplex: Full with switch selectable echo/no-echo
Data: 7 or 8 (switch selectable)
Stop Bits: 1 or 2 (switch selectable)
Parity: Switch selectable on transmit for odd, even, mark, space or disabled. (Parity transmitted but not tested)
Baud Rates: 110, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600 and 19200 (switch selectable)
Terminator: Switch selectable CR, LF, CR-LF or LF-CR.
Control: Supports Clear t Send (CTS), Request to Send (RTS) and switch selectable XON/XOFF.
Serial I/O Buffers: 4000 Characters each
Output Voltage: +/- 3.5 volts minimum (RL = 3K ohms)
Input Voltage: +/- 3.0 volts minimum: +/- 15 volts maximum
Connector: 25-Pin Sub-D male: DCE configured

IEEE 488-1978 Interface

SH1, AH1, T6, TEO, L4, LEO, SR1, PPO, RLO, DC1, CO, E1
Terminator: Switch selectable CR, LF, CR-LF, LF-CR with EOI
Connector: Standard Amphenol 57-20240 with metric studs

General

Indicators:	LEDs for Talk, Listen, Send, Receive and Power
Power:	1Ø5-125 [USA]; 6Ø Hz or 21Ø-25Ø [European]; 5Ø Hz; 7 VA MAX.
Power Supply Requirements:	1A, 9 volts
Current Draw:	.5A
Mean Time Between Failures:	4Ø,ØØØ hrs.
Environment:	Ø to 35'C; Ø to 7Ø% RH.
Dimensions:	19Ømm deep x 138mm wide x 68mm high (7.5" x 5.4" x 2.7")
Weight:	1.1kg (2.5 lbs)
Controls:	Power Switch (rear panel). Internal DIP switches for RS-232C and IEEE variables.

1.3 ABBREVIATIONS

The following IEEE 488 abbreviations are used throughout this manual.

addr n	IEEE bus address "n"
ATN	Attention line
CA	Controller Active
CO	Controller
CR	Carriage Return
data	Data String
DCL	Device Clear
GET	Group Execute Trigger
GTL	Go to Local
LA	Listener Active
LAG	Listen Address Group
LF	Line Feed
LLO	Local Lock Out
MLA	My Listen Address
MTA	My Talk Address
PE	Peripheral
PPC	Parallel Poll Configure
PPU	Parallel Poll Unconfigure
SC	System Controller
SDC	Selected Device Clear
SPD	Serial Poll Disable
SPE	Serial Poll Enable
SRQ	Service Request
TA	Talker Active
TAD	Talker Address
TCT	Take Control
term	Terminator
UNL	Unlisten
UNT	Untalk
*	Unasserted

SECTION 2

GETTING STARTED

2.1 INSPECTION

The Interface Converter was carefully inspected, both mechanically and electrically, prior to shipment. When you receive the interface, carefully unpack all items from the shipping carton and check for any obvious signs of physical damage which may have occurred during shipment. Immediately report any such damage found to the shipping agent. Remember to retain all shipping materials in the event that shipment back to the factory becomes necessary.

2.2 CONFIGURATION

Three DIP switches internal to the Interface Converter set the configuration of the interface.

> NOTE
>
> Most selectable functions are read ONLY at power-on and should only be set prior to applying power to the interface. The following figures illustrate the factory default conditions which are:

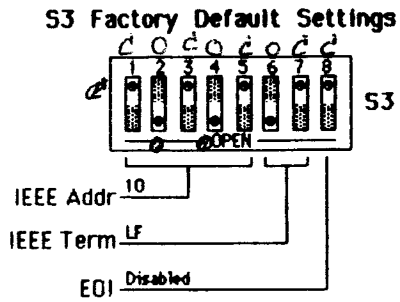
<u>Serial Port:</u>

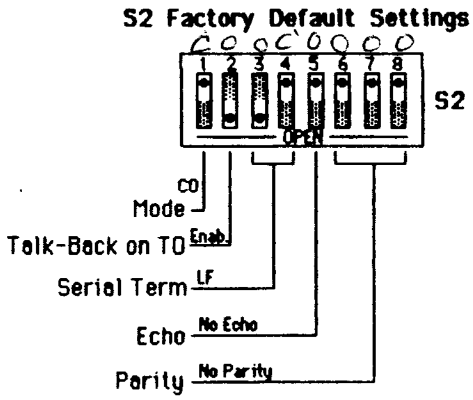
9600 Baud - No Parity
8 Data Bits
2 Stop Bits
Terminator = LF
XON/XOFF Disabled
Echo Disabled

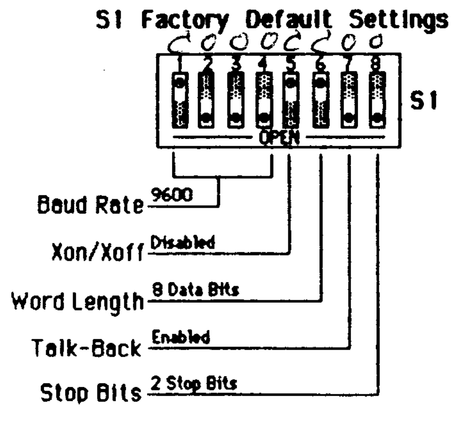
<u>IEEE:</u>

Mode = IEEE 488 Controller
Address = 10
Terminator = LF, EOI Disabled
Talk-Back on TE Enabled
Talk-Back on TO Enabled

FACTORY DEFAULT SETTINGS







Note that the Interface Converter comes configured as an IEEE controller. In this mode the Interface Converter is designed to allow an RS-232 computer to communicate with an IEEE peripheral such as a plotter. The Interface Converter may also be configured as an IEEE peripheral. As an IEEE peripheral the Interface Converter allows an IEEE controller or computer to communicate with RS-232 peripherals. For more details about these modes refer to Section 2.2.6.

To modify any of these defaults, follow this simple procedure: Disconnect the power supply from the AC line and from the interface. Disconnect any IEEE or serial cables prior to disassembly.

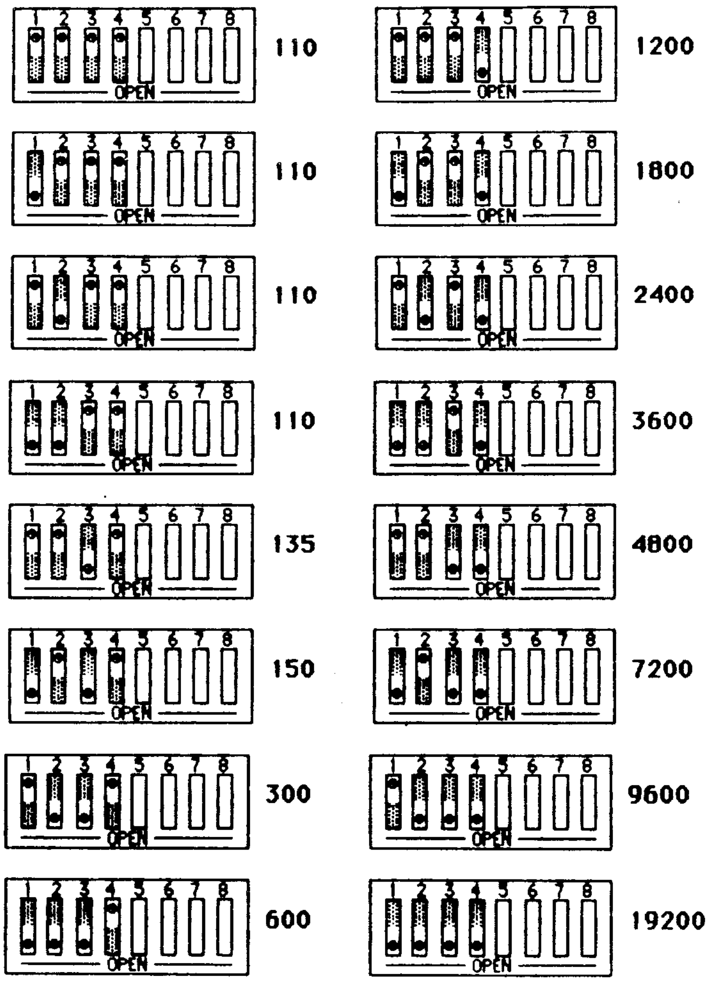
WARNING
Never open the Interface Converter case while it is connected to the AC line. Failure to observe this warning may result in equipment failure, personal injury or death.

Place the interface upside down on a flat surface. Remove the four (4) screws located near the rubber feet. Return the interface to the upright position and carefully remove the top cover. Modify those parameters which are appropriate for your installation and then carefully re-assemble the interface using the reverse of the procedure described.

2.2.1 SERIAL BAUD RATE SELECTION

S1-1 through S1-4 determine the serial baud rate. The factory default is 9600 baud. The baud rate may be selected from 110 to 19200.

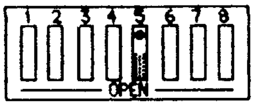
S1 VIEW FOR SERIAL BAUD RATE SELECTION



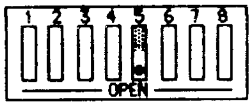
2.2.2 XON/XOFF SERIAL CONTROL SELECTION

Switch S1-5 is used to enable XON/XOFF serial control. When enabled, the Interface Converter issues XOFF when its serial input buffer is full. When it is able to accept more information it issues XON. The Interface Converter also accepts XON/XOFF on transmit from the serial device it is communicating with. RTS/CTS serial control will remain active even if XON/XOFF is enabled. The CTS input of the Interface Converter should be wired to the +V test if it is not used. The factory default is XON/XOFF disabled.

S1 View for XON/XOFF Serial Control



Xon/Xoff Disabled

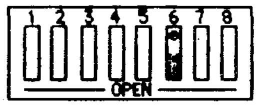


Xon/Xoff Enabled

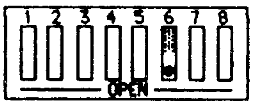
2.2.3 SERIAL WORD LENGTH SELECTION

S1-6 determines the number of bits per each serial character transmitted or received. The factory default is 8 data bits.

S1 View of Serial Word Length (Data Bits)



8 Data Bits

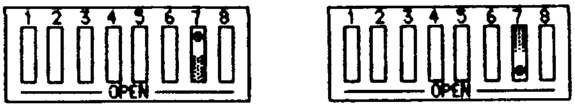


7 Data Bits

2.2.4 PERIPHERAL (PE) SRQ ENABLE/ CONTROLLER (CO) TALK-BACK ON TE ENABLE

The function of switch S1-7 depends on the current operating mode of the Interface Converter (see Section 2.2.6). In the IEEE Peripheral (IEEE 488 to RS-232C) mode it enables the interface to assert the SRQ IEEE bus interface line to indicate that it has received data from the serial device. In the IEEE Controller (RS-232C to IEEE 488) mode it is used to determine whether the interface should, after sending the IEEE Bus Terminators (TE), address the attached bus device to talk. Refer to Section 2.2.6 for a more complete description of these modes and features. The factory default is Talk-Back enabled.

S1 VIEW FOR PE SRQ AND CO TALK-BACK ON TE ENABLE

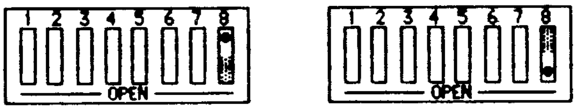


PE	**SRQ Disabled**	**SRQ Enabled**
CO	**Talk-back Disabled**	**Talk-back Enabled**

2.2.5 SERIAL STOP BIT SELECTION

Switch SW1-8 determines the number of stop bits contained in each serial character transmitted and received. The factory default is 2 stop bits.

SW1 VIEW FOR SERIAL STOP BIT SELECTION

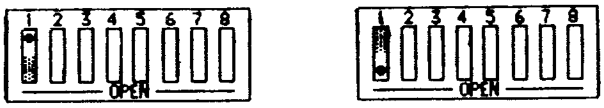


1 Stop Bit **2 Stop Bits**

2.2.6 MODE SELECTION

S2-1 sets the major operating mode of the Interface Converter, either IEEE Peripheral mode, or IEEE Controller mode. The factory default is the IEEE Controller mode.

S2 VIEW FOR MODE SELECTION



IEEE Controller **IEEE Peripheral**

2.2.6.1 IEEE CONTROLLER MODE

The IEEE Controller mode allows a serial host device to send data to a single IEEE bus peripheral. Applications include interfacing a listen-only or addressable IEEE printer/plotter to a serial printer port.

The IEEE device address is set with S3-1 through S3-5 [Refer to Section 2.2.11]. These switches set the address of the IEEE device that will be controlled, not the address of the Interface Converter. The address of the Interface Converter is automatically adjusted so that address conflicts will not occur.

Once the Interface Converter has initialized itself after power-on, it addresses the selected IEEE device to listen with the following bus sequence:

ATN@MTA,UNL,LAG,*ATN

Note that the IEEE bus device must be ready before the Interface Converter is turned on. Otherwise, the IEEE bus device will not receive the listen sequence, and the Interface Converter will be unable to communicate with it.

The data received from the serial host is placed into a circular serial input buffer. Simultaneously, characters are removed from that buffer and sent to the IEEE bus device. The serial terminator(s), if present, [as described in Section 2.2.8] are not sent. Instead, the IEEE terminators [as described in Section 2.2.12] are sent in their place.

So long as the serial input buffer is not empty the Interface Converter will continue to send data from it to the IEEE bus device. If the serial input buffer is emptied, then, if enabled, the Interface Converter will command the IEEE bus device to talk. This feature allows the Interface Converter to be used as a controller with devices, such as plotters, that return status and other information to the host computer.

When the serial input buffer becomes empty the Interface Converter checks the last characters sent to the IEEE bus device. If these were the IEEE bus terminators, the Talk-Back on Terminator [Section 2.2.4] is enabled and the IEEE bus device is addressed to talk. If the characters were not the IEEE bus terminators, the Talk-Back on Time-Out is enabled and the Interface converter waits 70 milliseconds. If no serial character has been received by then, the IEEE bus device is addressed to talk. The choice of talk-back modes depends strongly on the type of device and software being used. For most plotter applications both Talk-Back on Terminator and Talk-Back on Time-Out should be enabled.

When the Interface Converter addresses the IEEE bus device to talk, it uses the following bus sequence:

ATN@UNL,MLA,TAG,*ATN

The Interface Converter then accepts data from the IEEE device and returns it to the host until the IEEE terminators are detected.

The IEEE bus terminators are replaced by the serial terminators and these are then sent to the host. If the IEEE device has been addressed to talk but does not respond or finish transmission by the time additional characters are received into the circular serial input buffer, the talk sequence will be aborted to allow additional serial information to be sent to the IEEE device.

A control diagram is included in Appendix D which outlines the control flow for the IEEE Controller mode.

2.2.6.2 IEEE PERIPHERAL MODE

This mode is useful in interfacing a serial device such as a printer to an IEEE controller. Data which is sent by the IEEE controller to the Interface Converter is transmitted out its serial port. Data received from the serial device is buffered by the Interface Converter until read by the IEEE Controller.

The Interface Converter can buffer approximately 4000 bytes of data in each direction. When the IEEE input buffer is full, the Interface Converter will refuse to accept more data from the IEEE controller by preventing completion of the bus handshaking sequences. When the serial input buffer is full it will refuse to accept more data by negating its RTS output and, if enabled, by sending XOFF.

The following methods may be used by the IEEE controller when outputting data to the Interface Converter:

If the controller does not mind waiting an indefinite time for the serial device to become ready, then the data can simply be sent to the Interface Converter. If the serial device stops accepting data, the bus controller will be held up by the Interface Converter until the serial device becomes ready again. This type of control might be appropriate in a single user environment.

If the controller is set to detect a time-out error, then it will do so if the serial device stays not-ready for long. The error can be used to alert the operator to the problem, such as a printer out of paper, so that it can be corrected. If the controller then restarts transmission exactly where it left off, no data will be lost.

Finally, if the controller must avoid waiting for the serial device, it can serial poll the Interface Converter. The most significant bit [DIO8] of the serial poll byte is set to a logic "1" when the IEEE input buffer is not empty. If it is not empty, the controller should avoid sending any more data to the Interface Converter. If this bit is a logic "0", then the serial device has accepted all previous data and the controller may send more.

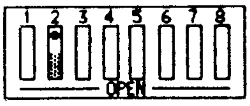
When data is sent by a serial device to the Interface Converter it is placed in a circular serial input buffer. When the serial terminator is received, DIO5 of the SPOLL byte is set to indicate to the IEEE controller that data has been received from the serial device. Once the data is read by the IEEE controller this bit is reset. If the PE SRQ switch [Refer to Section 2.2.4] is enabled, the Interface Converter will assert the IEEE bus SRQ line and set bit DIO7. The IEEE controller must perform a serial poll on the interface to clear the SRQ.

Note that data sent from the serial device must be terminated by the serial terminator(s) to be recognized. Also, the Interface Converter must be configured to respond to those terminators. The choice of appropriate terminators may be determined by inspection of the serial device instruction manual.

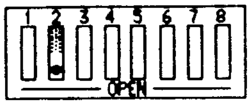
2.2.7 CONTROLLER TALK-BACK ON TIME-OUT (TO) ENABLE

Switch 2-2 selects whether, in the IEEE Controller (RS-232 to IEEE 488) mode, the Interface Converter should address the attached bus device to talk when the Interface converter has nothing more to send. Refer to Section 2.2.6 for details.

S2 View for CO Talk-Back on Time-Out Enable



Talk-Back Disabled

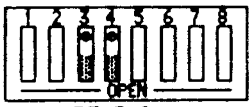


Talk-Back Enabled

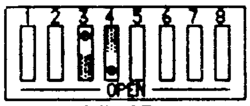
2.2.8 SERIAL TERMINATOR SELECTION

S2-3 and S2-4 select the serial terminators for the serial input and output. The factory default is LF.

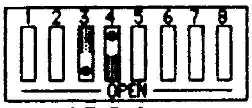
S2 View for Serial Terminator



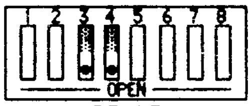
CR Only



LF-CR



LF Only

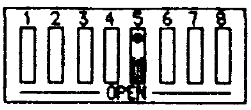


CR-LF

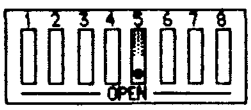
2.2.9 SERIAL ECHO SELECTION

Serial data sent to the Interface Converter will be echoed back if S2-5 is set to the open position. Factory default is Echo Disabled.

S2 View for Echo



Echo Disabled

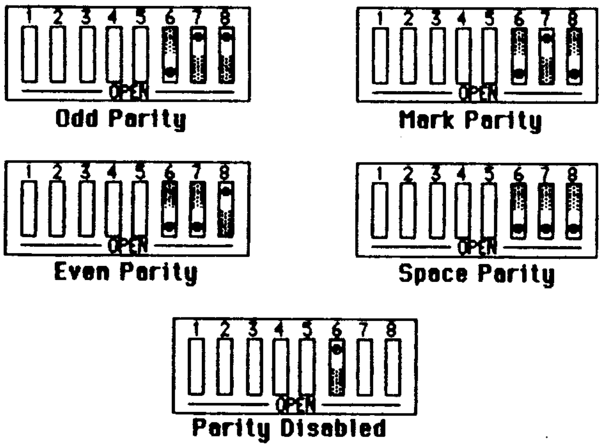


Echo Enabled

2.2.10 SERIAL PARITY SELECTION

Serial Parity is selected with S2-6 through S2-8. The Interface Converter generates the selected parity during serial transmissions but it does not check parity on data received. The factory default is parity disabled.

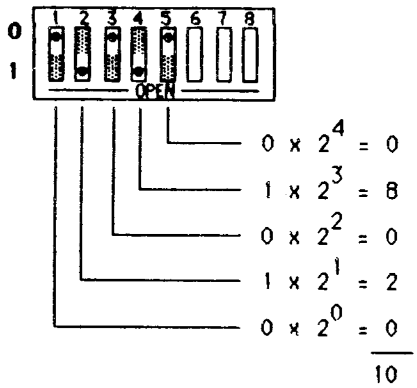
S2 View for Serial Parity Selection



2.2.11 IEEE ADDRESS SELECTION

S3-1 through S3-5 select the IEEE bus address of the Interface Converter when in the IEEE Peripheral mode. These same switches are used in the IEEE Controller mode to select the address of the device that will be controlled. [Refer to Section 2.2.6.1]. The address is selected by simple binary weighting with S3-1 being the least significant bit and S3-5 the most significant. The factory default is address 10.

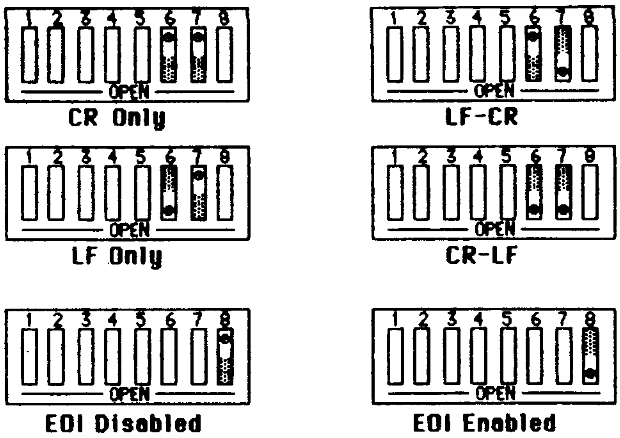
S3 View for IEEE Bus Address Selection



2.2.12 IEEE BUS TERMINATOR SELECTION

S3-6 through S3-8 set the IEEE bus terminators used for data sent or received by the Interface Converter. Factory default is LF with EOI disabled.

S3 View for IEEE Bus Terminators



2.3 OPERATION

After setting the defaults of the Interface Converter and reassembly of the unit, plug the power supply connector into the rear jack on the interface.

CAUTION
Never install the power supply into the interface while it is connected to AC line power. Failure to observe this caution may result in damage to the Interface Converter.

WARNING
The power supply provided with the interface is intended for INDOOR USE ONLY. Failure to observe this warning could result in equipment failure, personal injury or death.

After installing the power supply connector into the interface, plug the power supply into AC line power. Place the rear panel power switch in the ON [1] position. All the front panel indicators should light for approximately one second while the Interface Converter performs an internal ROM and RAM self check At the end of this self check all indicators except POWER should turn off.

If any of the lights remain lit a self-check error has occurred. In this case the SEND light indicates a ROM checksum error and the RECEIVE light indicates a RAM error. Should such an error occur, turn the rear panel switch to the OFF [Ø] position and retry the above procedure.

If the front panel indicators do not flash and the POWER indicator does not remain lit there may not be any power supplied to the interface. In this event, check the AC line and the rear panel connection of the power supply for proper installation. If the problem is unresolved, refer to the Service Information section of this manual.

If proper operation is obtained, connect an interface cable to the rear of the Interface Converter [25-Pin Sub-D]. Connect the other end to the host's serial port. Except for connecting IEE bus instruments, the Interface Converter is installed and ready to use.

WARNING
The Interface Converter makes its earth ground connection through the serial interface cable. It should only be connected to IEEE bus devices after being first connected to the host. Failure to do so may allow the Interface Converter to float to a bus device test voltage. This could result in damage to the interface, personal injury or death.

SECTION 3

IEEE 488 PRIMER

3.1 HISTORY

The IEEE 488 bus is an instrumentation communication bus adopted by the institute of Electrical and Electronic Engineers in 1975 and revised in 1978. The Interface Converter conforms to this most recent revision designated IEEE 488-1978.

Prior to the adoption of this standard, most instrumentation manufacturers offered their own versions of computer interfaces. This placed the burden of system hardware design on the end user if his application required the products of several different manufacturers. The popularity of the IEEE 488 interface (sometimes called the General Purpose Interface Bus or GPIB) is due to the total specification of electrical, mechanical, data transfer and control. This moved the responsibility of the user from system hardware design to high level software that was specific to the measurement application.

3.2 GENERAL STRUCTURE

The main purpose of the GPIB is to transfer information between two or more devices. A device can either be an instrument or a computer. Before any information transfer can take place it is first necessary to determine who will do the talking and who will be allowed to listen. The decision of who will talk and who will listen usually falls on the system controller.

The system controller is similar to a committee chairman. On a committee, only one person may speak at a time and the chairman is responsible for recognizing members and allowing them to have their say. On the bus, the device which is recognized to speak is the active talker. There can only be one talker at a time if the information transferred is to be clearly understood by all. The act of "giving the floor" to that device is called addressing to talk. If the committee chairman can not attend the meeting, or if other matters require his attention, he can appoint an acting chairman to take control of the proceedings. For the GPIB, this device becomes the active controller.

At a committee meeting, everyone present usually listens. This is not the case with the GPIB. The controller selects which devices will listen and commands all other devices to ignore what is being transmitted. A device is instructed to listen by being addressed to listen. This device is then referred to as an active listener. Devices which are to ignore the data message are instructed to unlisten.

The reason some devices are instructed to unlisten is quite simple. Suppose a college instructor is presenting the day's lesson. Each student is told to raise his hand if the instructor has exceeded his ability to keep up while taking notes. If hand is raised, the instructor stops his discussion to allow the slower student time to catch up. In this way, the instructor is certain that each and every student receives all the information he is trying to present. Since there are many students in the classroom, this exchange of information can be very slow. In fact, the rate of information transferred is no faster than the slowest note-taker can keep up. A particular student may have a question about the instructor's presentation which is of no interest to the rest of the class. The instructor tells the rest of the class to ignore his answer (unlisten) and answers the question at a rate in which the one student can take notes. This information transfer can then happen much quicker.

The GPIB transfers information in a similar way. This method of data transfer is called handshaking.

For data transfer on the IEEE 488, the active controller must...

1. Unlisten all devices to protect against eavesdroppers.
2. Designate who will talk by addressing a device to talk.
3. Designate all the devices who are to listen by addressing those devices to listen.
4. Indicate to all devices that the data transfer can take place.

IEEE 488 Bus Structure

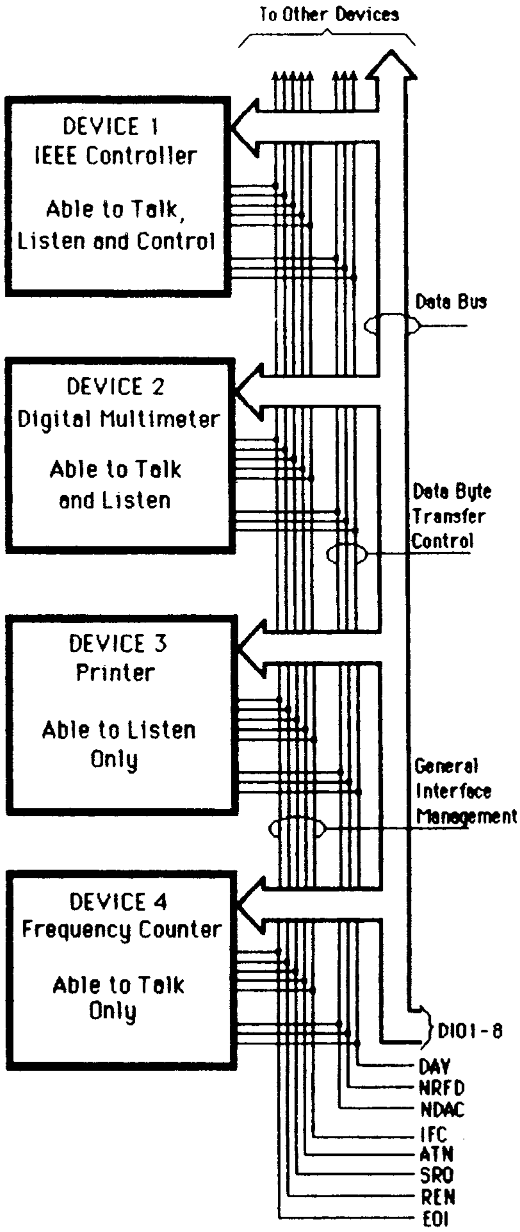


Figure 3.1

3.3 SEND IT TO MY ADDRESS

In the previous discussion, the terms addressed to talk and addressed to listen were used. These terms require some clarification as to what they refer to.

The IEEE 488 standard permits up to 15 devices to be configured within one system. Each of these devices must have a unique address to avoid confusion. In a similar fashion, every building in town has a unique address to prevent one home from receiving another home's mail. Exactly how each device's address is set is specific to the product's manufacturer. Some are set by DIP switches in hardware, others by software. Consult the manufacturer's instructions to determine how to set the address.

Addresses are sent with universal (multiline) commands from the system or active controller, such as My Listen Address (MLA), My Talk Address (MTA), Talk Address Group (TAG) and Listen Address Group (LAG).

3.4 BUS MANAGEMENT LINES

Five hardware lines on the GPIB are used for bus management. The associated commands these lines represent are often referred to as uniline (single line) commands.

3.4.1 ATN (ATTENTION)

ATN is one of the most important lines for bus management. Its state determines whether the information contained on the data lines is to be interpreted as data or as a multiline address or command. The active controller is the only bus device that has control of this line.

3.4.2 IFC (INTERFACE CLEAR)

The IFC line is used only by the system controller. It is used to place all bus devices in a known state. Although device configurations vary, the IFC command usually places the devices in the talk and listen idle states.

3.4.3 REN (REMOTE ENABLE)

When the controller sends the REN command, the device will respond to remote operation. Generally, the REN command should be issued before any bus programming is attempted. Only the system controller has control of the remote enable line.

3.4.4 EOI (END OR IDENTIFY)

The EOI line is used to signal the last byte of a multibyte data transfer. The device that asserts EOI depends on the direction of data flow. This line is also used by the active controller to perform a parallel poll.

3.4.5 SRQ (Service Request)

When a device desires the immediate attention of the controller, it asserts SRQ. It is then the controller's responsibility to determine which device requested service. This is accomplished with a serial poll or a parallel poll.

3.5 HANDSHAKE LINES

The GPIB uses three handshake lines in an "I'm ready - Here's the data - I've got it" sequence. This handshake protocol assures reliable data transfer, even at a rate determined by the slowest listener. One line is controlled by the talker, while the other two are shared by all active listeners.

3.5.1 DAV (DATA VALID)

The DAV line is controlled by the talker. The talker outputs data on the bus and waits until NRFD is unasserted which indicates that all addressed listeners are ready to accept the information. At the same time, the talker also verifies that NDAC is asserted which indicates that all listeners have accepted the previous data byte transferred. If these conditions are not met, the talker must wait until the NRFD and the NDAC lines are in the proper state. Once in the proper state, the talker asserts DAV to indicate that the data on the bus is valid.

3.5.2 NRFD (NOT READY FOR DATA)

This line is used by the listeners to inform the talker when they are ready to accept new data. Each listener must unassert this line and will do so at its own rate. This assures that all devices that are to accept the information are ready to receive it.

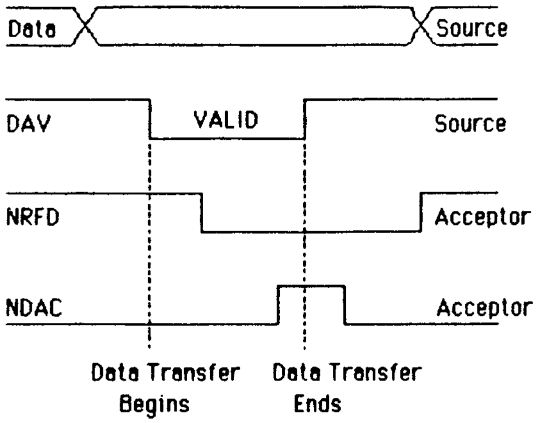
3.5.3 NDAC (NOT DATA ACCEPTED)

The NDAC line is also controlled by the listeners. This line indicates to the talker that each device addressed to listen has accepted the information. Each device releases NDAC at its own rate, but the NDAC will not go high until the slowest listener has accepted the data byte.

3.6 DATA LINES

The GPIB provides eight data lines for a bit parallel/byte serial data transfer. These eight data lines use the convention of D1Ø1 through D1Ø8 instead of the binary designation of DØ to D7. The data lines are bi-directional and are active low.

Handshake Process



3.7 MULTILINE COMMANDS

Multiline (bus) commands are sent by the active controller over the data bus with ATN asserted. These commands include addressing commands for talk, listen, untalk and unlisten.

3.7.1 GTL (GO TO LOCAL)

This command allows the selected devices to be manually controlled. [$Ø1]

3.7.2 LAG (LISTEN ADDRESS GROUP)

There are 31 (Ø to 3Ø) listen addresses associated with this group. The 3 most significant bits of the data bus are set to Ø11 while the 5 least significant bits are the address of the device being told to listen.

3.7.3 UNL (UNLISTEN)

This command tells all bus devices to unlisten. Also known as unaddressed to listen. [$3F]

3.7.4 TAG (TALK ADDRESS GROUP)

There are 31 (0 to 30) talk addresses associated with this group. The 3 most significant bits of the data bus are set to 101 while the 5 least significant bits are the address of the device being told to talk.

3.7.5 UNT (UNTALK)

This command tells bus devices to untalk. A more accurate phrase is unaddressed to talk. [$5F] –

3.7.6 LLO (LOCAL LOCKOUT)

Issuing the LLO command prevents manual control of the instrument's functions. [$11] DC1

ctrl.Q

3.7.7 DCL (DEVICE CLEAR)

This command causes all bus devices to be initialized to a predefined or power up state. [$14]

ctrl.T

3.7.8 SDC (SELECTED DEVICE CLEAR)

This causes a single device to be initialized to a predefined or power up state. [$04]

ctrl.D

3.7.9 SPD (SERIAL POLL DISABLE)

The SPD command disables all devices from sending their SERIAL POLL status byte. [$19]

ctrl.Y

3.7.10 SPE (SERIAL POLL ENABLE)

A device which is addressed to talk will output its SERIAL POLL status byte after SPE is sent and ATN is unasserted. [$18]

ctrl X

3.7.11 GET (GROUP EXECUTE TRIGGER)

This command usually signals a group of devices to begin executing a triggered action. This allows actions of different devices to begin simultaneously. [$08]

ctrl.H

3.7.12 TCT (TAKE CONTROL)

This command passes bus control responsibilities from the current controller to another device which has the ability to control. [$Ø9]
ctrl.I

3.7.13 SCG (SECONDARY COMMAND GROUP)

This indicates that one of the 32 possible commands (Ø to 31) in this group will follow. They must immediately follow a talk or listen address. [$6Ø to $7F]

3.7.14 PPC (PARALLEL POLL CONFIGURE)

This configures devices capable of performing a parallel poll as to which data bit they are to assert in response to a Parallel Poll. [$Ø5]
ctrl.E

3.7.15 PPU (PARALLEL POLL UNCONFIGURE)

This disables all devices from responding to a parallel poll. [$15]
ctrl.u

3.8 MORE ON SERVICE REQUESTS

Most of the commands covered, both uniline and multiline, are the responsibility of the controller to send and the bus devices to recognize. Most of these happen routinely by the interface and are totally transparent to the system programmer. Other commands are used directly by the user to provide optimum system control. Of the uniline commands, SRQ is very important to the test system and the software designer has easy access to this line by most devices. Service Request is the method by which a bus device can signal to the controller that an event has occurred. It is similar to an interrupt in a microprocessor based system.

Most intelligent bus peripherals have the ability to assert SRQ. A DMM might assert it when its measurement is complete, if its input is overloaded, or for any of an assortment of reasons. A power supply might SRQ if its output has current limited. This is a powerful bus feature that removes the burden from the system controller to periodically inquire, "Are you done yet?". Instead, the controller says. "Do what I told you to do and let me know when you're done" or "Tell me when something is wrong".

Since SRQ is a single line command, there is no way for the controller to determine which device requested the service without additional information. This information is provided by the multiline commands for serial poll and parallel poll.

3.8.1 SERIAL POLL

Suppose the controller receives a service request. For this example, let's assume there are several devices which could assert SRQ. The controller issues an SPE (serial poll enable) command to each device sequentially. If any device responds with DlØ7 asserted it indicates to the controller that it was the device that asserted SRQ. Often times the other bits will indicate why the device wanted service. This serial polling sequence, and any resulting action, is under control of the software designer.

3.8.2 PARALLEL POLL

The parallel poll is another way the controller can determine which device requested service. It provides the who but not necessarily the why. When bus devices are configured for parallel poll, they are assigned one bit on the data bus for their response. By using the Status bit, the logic level of the response can be programmed to allow logical OR/AND conditions on one data line by more than one device. When SRQ is asserted, the controller (under user's software) conducts a parallel poll. The controller must then analyze the eight bits of data received to determine the source of the request. Once the source is determined, a serial poll might be used to determine the why.

Of the two polling types, the serial poll is the most popular due to its ability to determine the who and why. In addition, most devices support serial poll only.

SECTION 4

SERVICE INFORMATION

4.1 THEORY OF OPERATION

At the heart of the Interface Converter is a 6809 microprocessor [U101] supported by 4K bytes of firmware ROM [U102 (2732)] and 8K bytes of static RAM [U103 (6264).] U118 (4020) is used to generate real time interrupts for the firmware operating system. The front panel annunciators are driven by an octal latch [U104 (74LS373)]. In addition, U104 provides software control of on board hardware.

The communications to and from the serial port are controlled by U105 (6551) through driver U114 (26LS30) and receiver U113 (26LS33).

IEEE 488 communications are controlled by U106 (9914A) through bus drivers/receivers U107 (75160A) and U108 (75162A).

Memory map decoding is accomplished by U109 (74LS139) along with U110 and U111. The memory map is set as follows:

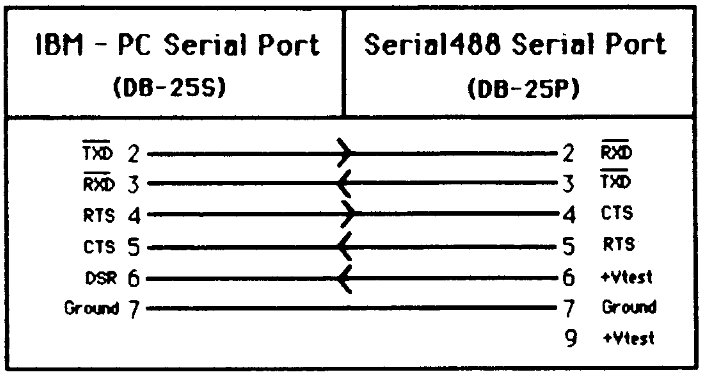
Address	Device	Part Number	Function
$A000 - $A007	U106	9914A	IEEE Controller
$A800 - $A803	U105	6551	UART
$B000	U104	74LS373	LED Driver
$C000 - $DFFF	U103	6264	Static RAM
$E000 - $FFFF	U102	2732	Program ROM

The DIP switches (S1, S2 and S3) are read at power-on through the octal bus transceivers U119, U120 and U121 respectively. Decoding for the drivers is accomplished by U122.

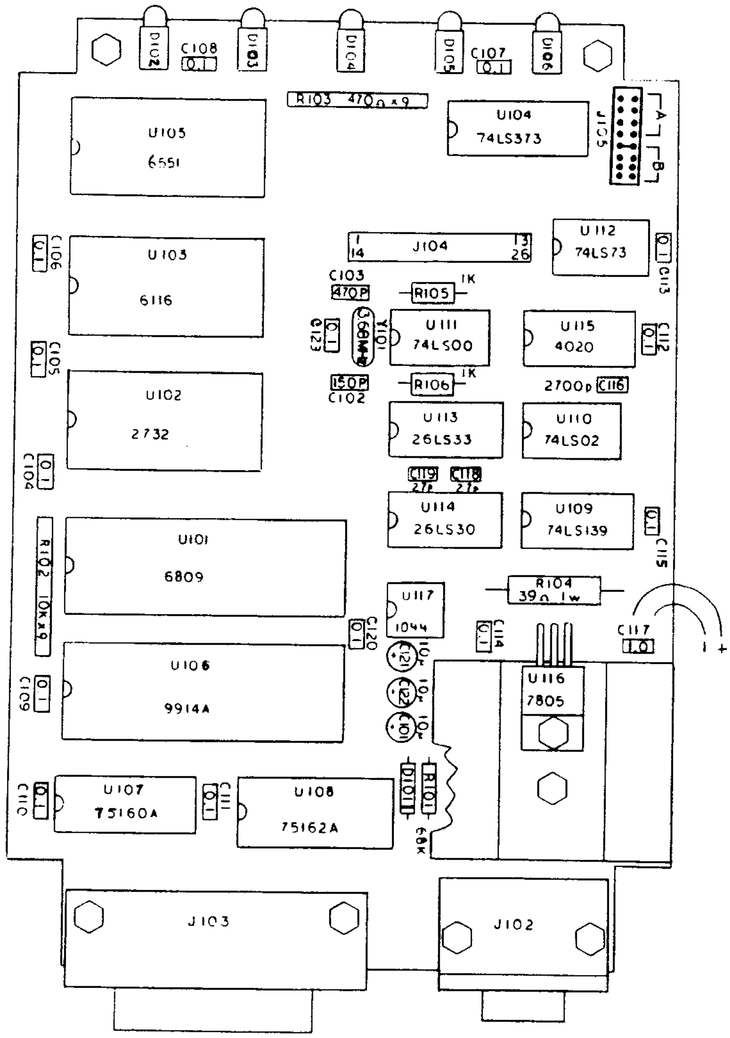
Power is supplied to the Interface Converter by an external AC to DC converter and applied through the rear panel power jack. The nominal output of this external unregulated supply is 9 volts DC. This is fed into the internal regulator [U116] to provide +5 volts to the interface. U117 (1044) is a power inverter and is used to generate the -5 volts DC required by the serial driver U114.

4.2 CONNECTOR WIRING DIAGRAM

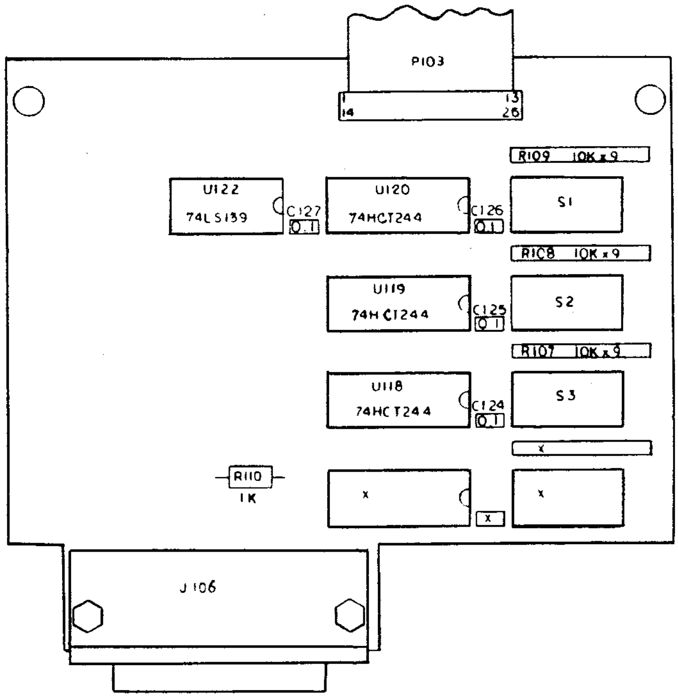
4.2.1 IBM-PC TO INTERFACE CONVERTER



4.3 INTERFACE CONVERTER COMPONENT LAYOUT (MOTHER BOARD)



4.4 INTERFACE CONVERTER COMPONENT LAYOUT (SWITCH BOARD)



4.5 INTERFACE CONVERTER PARTS LIST

Schematic	Description
C101	10uF, 25v electrolytic
C102	150pF, ceramic
C103	470pF, ceramic
C104	0.1uF, 25v ceramic
C105	0.1uF, 25v ceramic
C106	0.1uF, 25v ceramic
C107	0.1uF, 25v ceramic
C108	0.1uF, 25v ceramic
C109	0.1uF, 25v ceramic
C110	0.1uF, 25v ceramic
C111	0.1uF, 25v ceramic
C112	0.1uF, 25v ceramic
C113	0.1uF, 25v ceramic
C114	0.1uF, 25v ceramic
C115	0.1uF, 25v ceramic
C116	2700pF, ceramic
C117	1uF, 25v ceramic
C118	27pF, ceramic
C119	27pF, ceramic
C120	0.1uF, 25v ceramic
C121	10uF, 25v electrolytic
C122	10UF, 25v electrolytic
C123	0.1uF, 25v ceramic
C124	0.1uF, 25v ceramic
C125	0.1uF, 25v ceramic
C126	0.1uF, 25v ceramic
C127	0.1uF, 25v ceramic
D101	1N914 diode
D102	LED, Dialight #550-2406
D103	LED, Dialight #550-2406
D104	LED, Dialight #550-2406
D105	LED, Dialight #550-2406
D106	LED, Dialight #550-2406
J101	Pwr Connector SWCR #712A
J102	Not Used
J103	IEEE Connector
J104	13 x 2 pin header
J105	Not Used
J106	Fem 25 pin SUB D
P101	Not Used
P102	Not Used
P103	26 conductor ribbon assy
R101	68K ohms, 1/4w, 10% carbon
R102	10K ohms x 9 SIP Network
R103	470 ohms x 9 SIP Network
R104	39 ohms, 1 W, 10% carbon

Schematic	Description
R1Ø5	1K ohms, 1/4w, 1Ø% carbon
R1Ø6	1K ohms, 1/4w, 1Ø% carbon
R1Ø7	1ØK ohms x 9 SIP Network
R1Ø8	1ØK ohms x 9 SIP Network
R1Ø9	1ØK ohms x 9 SIP Network
R11Ø	1K ohms, 1/4w, 1Ø% carbon
S1Ø1	Power Switch
S1	8-pole DIP switch
S2	8-pole DIP switch
S3	8-pole DIP switch
U1Ø1	MC68Ø9B Microprocessor
U1Ø2	MBM2732-45 EPROM
U1Ø3	HM6264P-15 8k x 8 CMOS RAM
U1Ø4	SN74LS373 Octal Latch
U1Ø5	R6551P ACIA
U1Ø6	TMS9914ANL IEEE Controller
U1Ø7	SN7516ØAN Driver
U1Ø8	SN75162N Driver
U1Ø9	SN74LS139N Dual Decoder
U11Ø	SN74LSØ2N Quad NOR Gate
U111	SN74LSØØN Quad NAND Gate
U112	SN74LS73N Dual J-K Flip Flop
U113	DS26LS33CN RS-422 Receiver
U114	DS26LS3ØCN RS-422 Driver
U115	MC14Ø2Ø Divider
U116	LM78Ø5CT +5 Regulator
U117	LinTech 1Ø44 Voltage Inverter
U118	74HCT244 Octal Buffer
U119	74HCT244 Octal Buffer
U12Ø	74HCT244 Octal Buffer
U121	Not Used
U122	SN74LS139N Dual Decoder
Y1Ø1	3.6864 MHz Crystal
	Power Supply; 115 volts AC
	Power Supply; 22Ø volts AC

APPENDIX A

ASCII CHARACTER CODES

Dec	Hex	CHR	Dec	Hex	CHR	Dec	Hex	CHR	Dec	Hex	CHR
00	00	NUL	32	20	SPACE	64	40	@	96	60	`
01	01	SOX	33	21	!	65	41	A	97	61	a
02	02	STX	34	22	"	66	42	B	98	62	b
03	03	ETX	35	23	#	67	43	C	99	63	c
04	04	EOT	36	24	$	68	44	D	100	64	d
05	05	ENQ	37	25	%	69	45	E	101	65	e
06	06	ACK	38	26	&	70	46	F	102	66	f
07	07	BEL	39	27	'	71	47	G	103	67	g
08	08	BS	40	28	(	72	48	H	104	68	h
09	09	HT	41	29	)	73	49	I	105	69	i
10	0A	LF	42	2A	*	74	4A	J	106	6A	j
11	0B	VT	43	2B	+	75	4B	K	107	6B	k
12	0C	FF	44	2C	,	76	4C	L	108	6C	l
13	0D	CR	45	2D	-	77	4D	M	109	6D	m
14	0E	SO	46	2E	.	78	4E	N	110	6E	n
15	0F	SI	47	2F	/	79	4F	O	111	6F	o
16	10	DLE	48	30	0	80	50	P	112	70	p
17	11	DC1	49	31	1	81	51	Q	113	71	q
18	12	DC2	50	32	2	82	52	R	114	72	r
19	13	DC3	51	33	3	83	53	S	115	73	s
20	14	DC4	52	34	4	84	54	T	116	74	t
21	15	NAK	53	35	5	85	55	U	117	75	u
22	16	SYN	54	36	6	86	56	V	118	76	v
23	17	ETB	55	37	7	87	57	W	119	77	w
24	18	CAN	56	38	8	88	58	X	120	78	x
25	19	EM	57	39	9	89	59	Y	121	79	y
26	1A	SUB	58	3A	:	90	5A	Z	122	7A	z
27	1B	ESCAPE	59	3B	;	91	5B	[	123	7B	{
28	1C	FS	60	3C	<	92	5C	\	124	7C	|
29	1D	GS	61	3D	=	93	5D	]	125	7D	}
30	1E	RS	62	3E	>	94	5E	^	126	7E	~
31	1F	US	63	3F	?	95	5F	_	127	7F	DEL

Dec = decimal Hex = hexadecimal CHR = character
LF = Line Feed CR = Carrage Return FF = Form Feed
DEL = Rubout

APPENDIX B

SAMPLE PROGRAMS

```
10    REM***    DUMB TERMINAL PROGRAM FOR THE Interface Converter
15    REM***      Running under IBM basica
20    REM***    This program allows direct interaction between the
25    REM***    IBM-PC and an IEEE 488 bus device through the
30    REM***    Interface Converter.  The Interface Converter
                must be configured as
35    REM***    the IEEE bus controller.
40    REM***
45    REM***
50    REM***
60    CLS
70    REM***    Set communications parameters of COM1 port
80    OPEN"COM1:9600,N,8,1,cs,ds"AS 1
90    REM***    Display characters from COM1
100   IFLOC(1) THEN PRINT INPUT$(LOC(1),1);
110   REM***    Transmit any available characters from the keyboard
120   K$=INKEY$
130   PRINT #1,K$;:PRINTK$;
140   GOTO 100
```

APPENDIX C

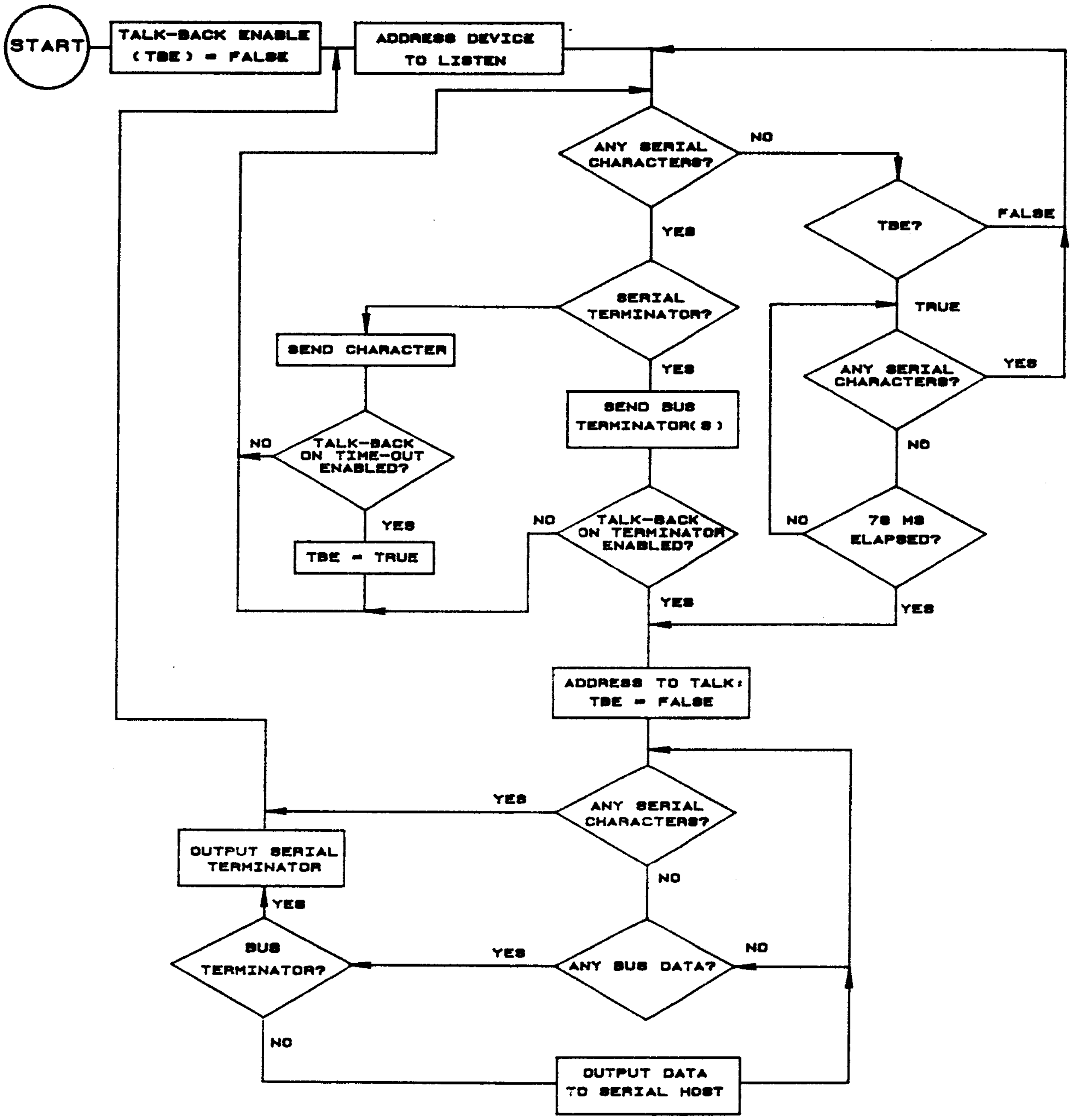
IEEE COMMAND AND ADDRESS MESSAGES

$00 0 NUL	$10 16 DLE	$20 32 SP 00	$30 48 0 16	$40 64 @ 00	$50 80 P 16	$60 96 ` SCG	$70 112 p SCG
$01 1 SOH GTL	$11 17 DC1 LLO	$21 33 ! 01	$31 49 1 17	$41 65 A 01	$51 81 Q 17	$61 97 a SCG	$71 113 q SCG
$02 2 STX	$12 18 DC2	$22 34 " 02	$32 50 2 18	$42 66 B 02	$52 82 R 18	$62 98 b SCG	$72 114 r SCG
$03 3 ETX	$13 19 DC3	$23 35 # 03	$33 51 3 19	$43 67 C 03	$53 83 S 19	$63 99 c SCG	$73 115 s SCG
$04 4 EOT SDC	$14 20 DC4 DCL	$24 36 $ 04	$34 52 4 20	$44 68 D 04	$54 84 T 20	$64 100 d SCG	$74 116 t SCG
$05 5 ENQ PPC	$15 21 NAK PPU	$25 37 % 05	$35 53 5 21	$45 69 E 05	$55 85 U 21	$65 101 e SCG	$75 117 u SCG
$06 6 ACK	$16 22 SYN	$26 38 & 06	$36 54 6 22	$46 70 F 06	$56 86 V 22	$66 102 f SCG	$76 118 v SCG
$07 7 BEL	$17 23 ETB	$27 39 ' 07	$37 55 7 23	$47 71 G 07	$57 87 W 23	$67 103 g SCG	$77 119 w SCG
$08 8 BS GET	$18 24 CAN SPE	$28 40 (08	$38 56 8 24	$48 72 H 08	$58 88 X 24	$68 104 h SCG	$78 120 x SCG
$09 9 HT TCT	$19 25 EM SPD	$29 41) 09	$39 57 9 25	$49 73 I 09	$59 89 Y 25	$69 105 i SCG	$79 121 y SCG
$0A 10 LF	$1A 26 SUB	$2A 42 * 10	$3A 58 : 26	$4A 74 J 10	$5A 90 Z 26	$6A 106 j SCG	$7A 122 z SCG
$0B 11 VT	$1B 27 ESC	$2B 43 + 11	$3B 59 ; 27	$4B 75 K 11	$5B 91 [27	$6B 107 k SCG	$7B 123 { SCG
$0C 12 FF	$1C 28 FS	$2C 44 , 12	$3C 60 < 28	$4C 76 L 12	$5C 92 \ 28	$6C 108 l SCG	$7C 124 ¦ SCG
$0D 13 CR	$1D 29 GS	$2D 45 - 13	$3D 61 = 29	$4D 77 M 13	$5D 93] 29	$6D 109 m SCG	$7D 125 } SCG
$0E 14 SO	$1E 30 RS	$2E 46 . 14	$3E 62 > 30	$4E 78 N 14	$5E 94 ^ 30	$6E 110 n SCG	$7E 126 ~ SCG
$0F 15 SI	$1F 31 US	$2F 47 / 15	$3F 63 ? UNL	$4F 79 O 15	$5F 95 _ UNT	$6F 111 o SCG	$7F 127 DEL SCG
ACG	UCG	LAG		TAG		SCG	

Note: ACG = Addressed Command Group
UCG = Universal Command Group
LAG = Listen Address Group
TAG = Talk Address Group
SCG = Secondary Command Group

APPENDIX D

CONTROLLER PASS-THRU DIAGRAM



NOTES

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